REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

Claims 1-14, 16, and 20-22 are pending in this application. Claim 18 is canceled by the present response without prejudice. Claim 18 was rejected under 35 U.S.C. §101, which rejection is now moot in view of the cancellation of Claim 18. Claims 1-14, 16, 18, and 20-22 were rejected under 35 U.S.C. §103(a) as unpatentable over U.S. patent 4,481,573 to Fukunaga et al. (herein "Fukunaga"). That rejection is traversed by the present response as discussed next.

Initially, applicant notes each of the independent claims is amended by the present response to clarify features recited therein. Specifically, independent claim 1 now recites "a plurality of functional units for performing functional processes". Independent claim 1 now also recites as a positive element a "storage means", additionally recites "second address translation means", and further clarifies that "the data virtual address space of said input/output registers and data are divided and disposed in a plurality of address areas so that the virtual addresses of an instruction and corresponding data and input/output registers are disposed at a near distance". The other independent claims are similarly amended as in independent claim 1.

The features recited in the amended claims are reflected for example in Figures 17-19 in the present specification. In those figures the functional units can correspond to one or plural of the signal processor unit 217, memory control unit 218, display control unit 220, JPEG encoder unit 223, and record control unit 224.

As recited in the claims, a plurality of functional units perform functional processes. Further, a storage device stores instruction and data for a processor to execute an operation and includes input/output registers for transferring the instructions and data between the processor and the functional units. The claims further recite a first address translation device

translating an instruction virtual address designated by a processor into a physical address of the storage, and a second address translating device translating a data virtual address including the virtual addresses of the data and the input/output registers designated by the processor into a physical address of the storage.

Thereby, as now clarified in the claims, two different address translation devices are provided. The first address translation device translates an instruction virtual address and the second translation device translates a data virtual address.

The features of such first and second address translation devices recited in the claims are believed to clearly distinguish over the teachings in Fukunaga.

The claims further recite, as previously recited, that the virtual address in the first virtual address space overlaps with the virtual addresses in the second virtual address base. The claims also further recite that the data virtual address space of the input/output registers and data are divided and disposed in a plurality of address areas so that the virtual addresses of an instruction and corresponding data and input/output registers are disposed at a near distance.

Those further features recited in the claims are believed to also clearly distinguish over Fukunaga.

The outstanding rejection appears to cite the prior art in Fukunaga at column 2, lines 56-61 as corresponding to the claimed features. At that portion Fukunaga discloses a pipelined controlled processor that has a unit for accessing an instruction and a separate unit for accessing an operand, and further including cache memories to attain a high speed operation. Fukunaga discloses that in such a prior art system each unit must have a translation lookaside buffer (TLB), and thereby hardware increases. The basis for the outstanding rejection indicates that such a device "may inherently map these otherwise independent virtual addresses associated with instructions and their corresponding operands

to a common physical address space along common boundaries if said TLBs correspondingly utilize common page/segment sizes and correspondingly utilize independent translation tables or means".[1]

In reply to the above-noted basis for the outstanding rejection, applicant notes the broad disclosure of a prior art pipelined controlled processor in Fukunaga is not at all directed to the claimed features. The claims recite specific operations of how first and second address translation devices interact with a storage device, which is neither taught nor suggested by Fukunaga. The claims also now clarify that a first address translation device has an operation for translating an instruction physical address and a second address translation device has a function for translating a data virtual address. Fukunaga does not disclose or suggest two separate address translation device with such dedicated different translating operations.

The claims also recite that the virtual address and the first virtual address space overlap with the virtual addresses of the second virtual address space. Fukunaga does not disclose that feature.

Moreover, the claims further recite that the virtual address space of the input/output registers, which are part of the storage device, and data are divided and disposed in a plurality of address areas so that the virtual addresses of an instruction and corresponding data and input/output registers are disposed at a near distance. Fukunaga does not disclose or suggest that further feature.

Thereby, applicant respectfully submits the claims as currently written positively recite features neither taught nor suggested by Fukunaga, and thus the claims as written are believed to overcome the outstanding rejection based on Fukunaga.

[1] Office Action of August 23, 2006, page 3, lines 8-12 of prenumbered paragraph 7.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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